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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Appeal and Interferences

In the application of	:	D J Stacey et al
Serial No.	:	09/416,679
Filed	:	October 12, 1999
For	:	ATM Common Part Sub-Layer Device and Method
Examiner	:	T L Lee
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Name of person signing: Kathy Kurek
Signature Kathy Kurek

BRIEF ON APPEAL

This appeal is from the Examiner's final Office Action of October 6, 2003. A timely Notice of Appeal was submitted to the Patent and Trademark Office, with an extension of time, on January 28, 2004.

This Brief is being submitted in triplicate, with the required fee of $330. Should any further charges be required, those charges may be deducted from Deposit Account 12-0913.

(1) **Real Party in Interest**

This application is assigned to Nortel Networks Corporation, who by change of name is now Nortel Networks Limited. Nortel Networks Limited is the real party in interest.

(2) **Related Appeals and Interferences**

There are no related appeals or interferences.

(3) **Status of Claims**

This application was filed with claims 1 through 17. Of the claims, claims 6 to 12 & 15 are pending as filed, claims 2, 3, 5, 14, 16 & 17 have been amended once and claims 1, 4 & 13 cancelled. Consequently, it is the rejection of claims 2, 3, 5 to 12 & 14 to 17 that is appealed. The claims (2, 3, 5 to 12 & 14 to 17) as currently pending are set forth in the Appendix.

(4) **Status of Amendments**

A paper entitled "Response to Office Action Mailed October 6, 2003" was filed November 28, 2003. No amendment of the claims was made. The Response was entered, and no further filing has been made after the Final Rejection.

(5) **Summary of Invention**

The present invention concerns a functional partitioning of an ATM common part sub-layer (CPS) adaptation device to enable different traffic services to be carried over different adaptation layers, for example AAL1,

AAL2 & AAL5, and to support AAL2 switching. A key requirement of any adaptation layer partitioning is that it optimizes buffering apportionment in order to minimize delays and to minimize the amount of memory resources employed and hence the cost of implementation (refer page 2, lines 20 to 32).

The present invention addresses this object by providing a **common part sublayer (CPS)** ATM adaptation device incorporating ingress and egress paths respectively to and from a broadband (ATM) network (see figures 5a and 5b). Buffer storage (memory) is required in the CPS ATM adaptation device ingress path for reasons of scheduling ATM cells to the ATM broadband network according to traffic class and priority and to control the assembly of AAL2 mini-packets into ATM CPS payload data units (PDUs) (refer page 8, lines 23 to 32). As such, the CPS ingress path has incorporated therein a common memory (primary buffer) for payload storage. In a preferred embodiment of the invention, an optional memory is incorporated into a service specific convergence sublayer (SSCS) (part of the) ingress path for reasons of storing fragmented SDUs etc although the present invention as defined by independent claims 2, 12, 16 & 17 is not limited to this feature.

In contrast to the CPS ingress path, the CPS egress path operates as a flow-through path, i.e. does not incorporate any memory (buffer) for payload storage purposes. In the preferred embodiment of the invention, a primary buffer is incorporated into a SSCS egress path but once again the present invention as defined by the currently pending independent claims is not limited to this feature.

One advantage of having the CPS egress path operate as a flow-through path is that, for AAL2 switching applications, traffic received on the CPS egress path can be immediately re-routed internally within the CPS ATM adaptation device onto the CPS ingress path without being delayed by unnecessary buffering in the CPS egress path. Such traffic will be buffered as necessary in the common memory (primary buffer) of the CPS ingress path to which it has just been re-routed prior to being re-transmitted on the ATM

broadband network. In the preferred embodiment of the invention incorporating a primary buffer in the SSCS egress path, traffic flowing through the CPS egress through path which has not been not switched to the CPS ingress path for re-transmission on the ATM network is buffered as necessary in the SSCS egress path prior to being disassembled.

(6) Issues

The following issue is presented:

The rejection of claims 2, 3, 5 to 12 & 14 to 17 as being obvious (under 35 U.S.C. §103(a)) over Westberg et al (US5946309) (hereinafter referred to as "Westberg '309") in view of Westberg (US6195353) (hereinafter referred to as "Westberg '353").

(7) Grouping of Claims

Claims 2, 3, 5 to 12 & 14 to 17 can be considered as a group.

(8) Argument

It is the Examiner's view that the currently pending independent claims 2, 12, 16 & 17 define an invention which would have been obvious over the combination of Westberg '309 and Westberg '353. The Examiner's position as set out in the last substantive office action mailed October 6, 2003 might be summarized as being that Westberg '309 generally teaches all the features of the independent claims with the exception of the scheduling or prioritization of ingress traffic (cf section 3 of the office action). This, the Examiner contends, is taught by Westberg '353 as confirmed by the Examiner's comments in section 13 of said action to the effect that "*Only the teachings relating to the scheduling and prioritization that involve the input buffer taught*

by Westberg ('353) *are being incorporated into the system of Westberg et al* ('309).".

Considering the teaching of Westberg '309 more fully, it can be seen that this teaches a new Hybrid AAL multiplexing scheme which is not compatible with the ATM standard that has been widely implemented worldwide. The disclosure of Westberg '309 is of a scheme by which ATM adaptation layers (AALs) 1, 5 and m, a precursor of AAL2, may share a single ATM virtual (not physical) channel connection (VCC), i.e. all ATM cells would carry the same VPI/VCI pair.

To perform this multiplex of payloads, control information must be sent to a receiving station to identify the format of all payloads explicitly, rather than implicitly as is done in systems implementing the ATM standard, for which there is normally only one AAL per VCC, i.e. the VPI/VCI pair implicitly provides the information. In Westberg '309, communications data and the corresponding control data are multiplexed into a single data stream which is then transmitted to a receiving station (cf abstract).

Westberg '309 teaches four methods of conveying the explicit control information:

1) re-use of a field (PTI) in the ATM header (which denies its standard use). This is done on a per cell basis and only encodes AAL type (one of four), but has no other means to convey further address information;

2) a new format for a Resource Management (RM) cell, which batches the control information to represent a sequence of ATM cells. That sequence is expressed in a run-length encoded form of: AAL type, number of payloads, and may carry an "AAL address" (but does not define any ATM address information). This batching requires buffering the entire sequence of ATM cells at the transmitter and receiver so that the control information can be generated/acted upon;

3) stealing an octet from an AALm payload to signify on a defacto AALm VCC that there follows intervening non-AALm cells and their number. This embodiment restricts the non-AAL to one type, has limited sequence length, and carries no other address information; and

4) a newly defined Resource Management (RM) minicell for embedding in an AALm stream to convey much the same information and format that was specified for the ATM RM cell version (2 above), with similar restrictions, as well as the connection having to be AALm defacto.

Since the system taught by Westberg '309 is not compatible with the ATM standard, it exhibits significant restrictions over standard compatible ATM systems such as:

a) No method is disclosed for sending any ATM address information for each of the several possible AAL types, so that each AAL is limited to a single address, i.e. all AALs are associated with a single pair of end stations;

b) The ATM cells of any given AAL type must be sent contiguously in several of the control methods, whereas they may be freely multiplexed in a standard ATM system;

c) The cell steam must be **buffered at the receiver** until the control information can be used to interpret the information, which is extra delay over standard ATM and requires a special control architecture not normally implemented in standard ATM systems; and

d) Any loss or corruption of control information, especially when using either RM method (2, 4) can cause a significant error extension, and no disclosure is made how the method may be made robust.

In contrast, the present invention is an ATM standard compatible system. The system of the present invention does not use any explicit control information sent between stations to perform multiplexing and de-multiplexing

operations and so does not require means for buffering such explicit control information at a receiving station.

Westberg '309 provides no teaching with respect to how to partition an ATM adaptation layer device as claimed in the present application. Furthermore, the buffering requirements for processing control information, particularly when processing RM cells or RM mini-cells, is contrary to that claimed in the present application where a CPS egress path is partitioned to be a flow-through path.

It should also be noted with respect to Westberg '309 that the communications channel is a virtual channel and relates to sharing a single VCC. Westberg '309 teaches this as a means of specifically avoiding using many ATM virtual connections. It would make no sense to infer sharing a physical connection as all the steps of the method taught by Westberg '309 would be obviated by the native capabilities of ATM.

Westberg does not explicitly mention buffering because the specification is incomplete. A person skilled in the art would recognize that a batch encoding of the control information sent infrequently would have to precede the user data to allow decoding with the result that this requires buffering on receipt. In contrast, the CPS egress path of the CPS adaptation device of the present invention is configured as a flow-through (non-buffered) path.

Referring now to Westberg '353, this teaches an application of ATM AAL2 for the specific purpose of a circuit emulation service, i.e. a fixed bit rate data stream. A bit stream is assembled into short packets (shorter than an ATM cell payload) whose length may be fixed or vary depending on the clocking arrangement. This arrangement is suitable for multiplexing into an AAL2 connection at the CPS layer. On receipt, the short packets of this service are de-multiplexed and the clock recovered in order to dismantle the packets again and reconstitute the bit stream. Where the bit stream is structured, a field may be added to the payload of the short packet to

delineate the boundary of the structure in relation to the short packet payload. Where the bit stream does not form an integral number of bytes, there may be a padding byte to state the number of and include a requisite number of padding bits.

This is a non-standard implementation of the ATM standard since this subject matter is not part of any ATM or AAL2 standards. There is no circuit emulation service in AAL2, only in AAL1. AAL2 has a structured transfer mode for 64kb/s channels (not normally considered low-bit rate) but the structure is fixed and always aligned with the packet boundary so no pointer is used.

In any event, the functions described in Westberg '353 only relate to what is now termed the service specific convergence sub-layer (SSCS). As such, Westberg '353 does not specify any CPS functionality and so, like Westberg '309, does not teach the functional partition of a CPS ATM adaptation device as claimed in the present application.

In as far as Westberg '353 might be said to allude to a CPS device, it does so as a black-box function, labelled 565, 625, 730 and 810 in the various diagrams thereof. However, it provides no teaching as to how this black box is implemented. There is no disclosure in Westberg '353 of short packet scheduling other than it is assumed to be "pre-programmed", with no teaching for dynamic scheduling priorities and state based according to connection type.

Since Westberg '353 pertains to a function of the ATM AAL2 SSCS layer, not the CPS layer, buffers supporting the SSCS operation do not apply to the operation of the multiplexing CPS layer as taught in the present application and as claimed therein.

To establish a prima facie case of obviousness, it is necessary to show that the prior art references teach or suggest all of the claim limitations. Neither Westberg '309 nor Westberg '353 teach the functional partitioning of a

common part sublayer ATM adaptation device. While Westberg '353 teaches a system that utilizes the ATM adaptation layer, it neither suggests nor even mentions the possibility that buffer apportionment can be addressed with respect to the common part sublayer (CPS) ingress and egress paths of the ATM adaptation layer. On this basis alone, the rejection under 35 U.S.C. §103(a) cannot be sustained.

Also, the Examiner has previously contended that, since Westberg '309 does not mention buffering the incoming data to the receiving station, it can be considered as a "through path". The applicants again contest this conclusion on the grounds that the complete absence in a prior art reference of any discussion of a feature as claimed in the invention cannot be said to have satisfied the test that the prior art reference teaches or suggests the feature. As already demonstrated in the foregoing, it is implicit to the teaching of Westberg '309 that control information must be buffered on receipt at a receiving station. At best, Westberg '309 can be said to be ambiguous with respect to this feature.

Issue is also taken with the Examiner's conclusion as to what Westberg '353 teaches. It is apparent from Westberg '353, col. 3, line 61 to col. 4, line 60, that there is provided an input buffer 530 for each circuit emulation connection 525 wherein the function of the input buffer 530 is to allow the operator, in association with a packetization clock period, to control the length of the short packets extracted from the input buffer 530 for that circuit 525 (col. 4, lines 17 to 20). Short packets from the input buffer 530 can then be multiplexed with short packets extracted from the input buffers 530 of other circuits 525. Consequently, Westberg does not teach the provision of a common memory for payload storage in the CPS ingress path in order to perform multiplexing at both the AAL and ATM layers. Therefore the rejection under 35 U.S.C. §103(a) cannot be sustained for this reason either.

Since claims 3, 5 to 11, 14 & 15 are dependent claims, the rejection of these claims under 35 U.S.C. §103(a) with respect to Westberg '309 and Westberg '353 is moot in view of the foregoing.

In conclusion, it has been demonstrated above that the Examiner's rejection of the claims under 35 U.S.C. §103 is in error, and must be reversed. Such action by the Board of Appeal and Interferences is therefore urged.

Respectfully submitted,

Date: 2/9/04

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APPENDIX

Claims

2. A common part sublayer (CPS) ATM adaptation device, for interfacing between a narrow band network and a broad band network said device being functionally partitioned to provide scheduling, prioritization and multiplexing of ingress traffic to the broadband network independently of the adaptation layer (AAL) type of that traffic, and incorporating ingress and egress paths respectively to and from the broadband network, wherein said egress path provides on a through path segregation and delineation of incoming data units on to respective external data ports, and wherein said ingress path incorporates a common memory for payload storage whereby to perform multiplexing at both AAL and ATM layers.

3. A common part sublayer ATM adaptation device as claimed in claim 2, and arranged to schedule a dispatch of cells or packets into an asynchronous network at a substantially constant rate.

5. A common part sublayer ATM adaptation device as claimed in claim 3, wherein said segregation on to external data ports is determined from a combination of connection identifier, call state and packet type.

6. A common part sublayer ATM adaptation device as claimed in claim 5, wherein said multiplexing is controlled by a scheduling and congestion avoidance mechanism.

7. A common part sublayer ATM adaptation device as claimed in claim 6, wherein said payload memory provides for the storage of AAL2 mini-packet SDUs and/or ATM cell SDUs.

8. A common part sublayer ATM adaptation device as claimed in claim 7, and arranged to provide an AAL2 and ATM switching function.

9. A common part sublayer ATM adaptation device as claimed in claim 7, and incorporating a service specific convergence sublayer so as to provide ATM and IP trunking and interworking functions.

10. A common part sublayer ATM adaptation device as claimed in claim 7, and having a shared memory for data in the ingress direction so as to provide buffer storage for said ingress data.

11. A common part sublayer ATM adaptation device as claimed in claim 10, and incorporating an ingress dynamic buffer whereby to provide quality of service (QoS) control.

12. A method of interfacing a narrow band network and a broadband network via a common part sublayer (CPS) ATM adaptation device, the method comprising; in an ingress direction towards the broadband network, providing scheduling, prioritization and multiplexing of ingress traffic to the broadband network independently of the adaptation layer (AAL) type of that traffic, and, in an egress direction from the broadband network, providing on a through path segregation and delineation of incoming data units.

14. A method as claimed in claim 12, wherein said segregation on to external data ports is determined from a combination of connection identifier, call state and packet type.

15. A method as claimed in claim 14, wherein said multiplexing is controlled by a scheduling and congestion avoidance mechanism.

16. A communications network arrangement, comprising a narrow band network, a broadband network, and a common part sublayer (CPS) ATM adaptation device providing an interfacing function therebetween, wherein common part sublayer ATM adaptation device is functionally partitioned to provide scheduling, prioritization and multiplexing of ingress traffic to the broadband network independently of the adaptation layer (AAL) type of that traffic, and incorporates ingress and egress paths respectively to and from the

broadband network, wherein said egress path provides on a through path segregation and delineation of incoming data units on to respective external data ports, and wherein said ingress path incorporates a common memory for payload storage whereby to perform multiplexing at both AAL and ATM layers.

17. Software in machine readable form for operating a common part sublayer (CPS) ATM adaptation device, for interfacing between a narrow band network and a broad band network, said software being adapted to functionally partition the device so as to provide scheduling, prioritization and multiplexing of ingress traffic to the broadband network independently of the adaptation layer (AAL) type of that traffic to provide scheduling, prioritization and multiplexing of ingress traffic to the broadband network independently of the adaptation layer (AAL) type of that traffic, and incorporating ingress and egress paths respectively to and from the broadband network, wherein said egress path provides on a through path segregation and delineation of incoming data units on to respective external data ports, and wherein said ingress path incorporates a common memory for payload storage whereby to perform multiplexing at both AAL and ATM layers.